CLAIMS

Please cancel claims 10, 38, 40-41, and 47 without prejudice or disclaimer. Please amend the claims as shown in the following claim listing:

1. (Currently amended) A method comprising:

checking a current clock period when a memory is accessed to read data, the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period during a writeback cycle to write the read data back to the memory, the usage bit indicating usage information for the ~~memory~~ read data.

2. (Currently amended) The method of claim 1, further comprising:

erasing usage bits corresponding to a new clock period ~~when the new clock period begins~~.

3. (Previously presented) The method of claim 2, wherein erasing includes erasing the usage bits at once.

4. (Previously presented) The method of claim 1, further comprising:

resetting usage bits in response to changing an address/tag of the memory; and

setting a usage bit corresponding to a current clock period.

5. (Original) The method of claim 1, wherein the memory is a non-volatile cache memory.

6. (Currently amended) The method of claim ~~5~~ 1, wherein the given number of clock periods is four.

7. (Canceled).

8. (Currently amended) The method of claim ~~5~~ 1, wherein the ~~non-volatile cache~~ memory is a destructive read memory.

9. (Original) The method of claim 8, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

10. (Canceled).

11. (Currently amended) The method of claim 1, further comprising:

de-allocating data in the memory based upon ~~the~~ usage bits ~~if the memory is considered full~~.

12. (Currently amended) A memory comprising:

an area to store data; and

an area to store metadata for the data, the metadata including:

a plurality of usage bits to indicate usage information for data in the memory, ~~each~~ a usage bit corresponding to one of a given number of clock periods, wherein the memory is a destructive read ~~cache~~ memory and wherein ~~the plurality of usage bits are~~ a usage bit for data read from the memory is updated during a writeback cycle to write the read data back to the memory.

13. (Original) The memory of claim 12, wherein the usage information is a least recently used information.

14. (Currently amended) The memory of claim 12, wherein the destructive read memory is a non-volatile cache memory.

15. (Currently amended) The memory of ~~claim 14, wherein~~ claim 12, wherein the given number of clock periods is four.

16. (Canceled).

17. (Previously presented) The memory of claim 12, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

18. (Currently amended) A system comprising:

a magnetic memory device;

a destructive read memory to cache data for the magnetic memory device and to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for data in the memory, ~~each~~ a usage bit corresponding to one of a given number of clock periods; and

a memory controller to update ~~the usage bits during a writeback cycle based on the clock period and~~ a usage bit for data read from the memory during a writeback cycle to write the read data back to the memory, the memory controller to de-allocate ~~the~~ data using the plurality of usage bits.

19. (Original) The system of claim 18, wherein the usage information is a least recently used information.

20. (Currently amended) The system of claim 18, wherein the destructive read memory is a non-volatile cache memory.

21. (Currently amended) The system of claim ~~20~~ 18, wherein the given number of clock periods is four.

22. (Canceled).

23. (Currently amended) A method comprising:

storing metadata comprising usage information for data in a memory; and

updating ~~the~~ usage information for data read from the memory during a writeback cycle to write the read data back to the memory.

24. (Original) The method of claim 23, wherein the usage information is a least recently used information.

25. (Previously presented) The method of claim 23, wherein storing includes storing usage bits to indicate the usage information.

26. (Currently amended) The method of claim 25, wherein updating ~~the~~ usage information comprises:

checking a current clock period when the memory is accessed to read data, the current clock period being one of a predetermined number of clock periods; and

setting a usage bit corresponding to the current clock period, the usage bit indicating usage information for the ~~memory~~ read data.

27. (Currently amended) The method of claim 26, ~~wherein updating the usage information further comprises:~~ comprising:

erasing usage bits corresponding to a new clock period ~~when the new clock period begins~~.

28. (Currently amended) The method of claim 26, ~~wherein updating the usage information further comprises:~~ comprising:

resetting usage bits when an address/tag of the metadata is changed; and

setting a usage bit corresponding to a current clock period.

29. (Currently amended) The method of claim ~~26~~ 23, wherein the memory is a non-volatile cache memory.

30. (Currently amended) The method of claim ~~29~~ 26, wherein the predetermined number of clock periods is four.

31. (Currently amended) The method of claim ~~29~~ 23, wherein the ~~non-volatile cache~~ memory is a destructive read memory.

32. (Currently amended) An instruction loaded in a machine readable medium comprising:

a first group of instructions to check a current clock period when a memory is accessed to read data, the current clock period being one of a predetermined number of clock periods; and

a second group of instructions to set a usage bit corresponding to the current clock period during a writeback cycle to write the read data back to the memory, the usage bit indicating usage information for the ~~memory~~ read data.

33. (Currently amended) The instruction of claim 32, further comprising:

a third group of instructions to erase usage bits corresponding to a new clock period ~~when the new clock period begins~~.

34. (Previously presented) The instruction of claim 32, further comprising:

a third group of instructions to reset usage bits for the memory in response to changing an address/tag of the memory, and to set a usage bit corresponding to a current clock period.

35. (Currently amended) An instruction loaded in a machine readable medium comprising:

a first group of computer instructions to store metadata information for ~~a line of~~ data in a memory, wherein the metadata information includes usage information; and

a second group of computer instructions to update ~~the~~ usage information for data read from the memory during a writeback cycle to write the read data back to the memory.

36. (Canceled).

37. (Currently amended) The instruction of claim 35, wherein the first group of computer instructions includes instructions to store metadata information for ~~a line of~~ data in a destructive read memory.

38. (Canceled).

39. (Canceled).

40. (Canceled).

41. (Canceled).

42. (Currently amended) An apparatus comprising:

a non-volatile destructive read memory to cache data for a storage device and to store usage information for the cache data stored in the non-volatile destructive read memory,

wherein usage information is updated during a writeback cycle to rewrite data destroyed during a read process back to the non-volatile destructive read memory.

43. (Previously presented) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric random access memory (PFRAM), a magnetic RAM (MRAM), or a core memory.

44. (Previously presented) The apparatus of claim 42, wherein the storage device is a magnetic or optical memory device.

45. (Previously presented) The apparatus of claim 42, further comprising:
a cache controller coupled to the non-volatile destructive read memory; and
a main memory coupled to the cache controller.

46. (Previously presented) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric memory.

47. (Canceled).

48. (Previously presented) The apparatus of claim 42, wherein the usage information is least recently used information.